

Exhibit 52

Low-latency Chip-to-Chip *and beyond* Interconnect[HOME](#)[Why HyperTransport](#)[Download Specifications](#)[Join The Consortium](#)**PRESSROOM**[Pressroom](#)[Press Releases](#)[News Articles](#)[Press Release Archives](#)[Images](#)[Quotes](#)**SEARCH**[Press Releases](#)[News Articles](#)[Online Press Room](#)[Press Release Archives](#)**Editor Contact:**[Joel Slatis](#)

PMC-Sierra, Inc.

For HyperTransport Consortium

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For Immediate Release**API NetWorks Accelerates Use of HyperTransport™ Technology With Launch of Industry's First HyperTransport Technology-to-PCI Bridge Chip****Chip Connects HyperTransport Bus to Wide Range of PCI Devices to Reduce Data Bottlenecks and Boost Performance of PCs and Communications Devices**

Concord, Mass., April 2, 2001 -- API NetWorks Inc. today announced the industry's first HyperTransport technology-to-PCI bridge chip, the AP1011, a key piece of technology that will accelerate the use of HyperTransport technology-based processors. Co-developed by AMD and API NetWorks, HyperTransport is a new high-speed bus that reduces data bottlenecks and boosts the performance of current and future PCs and communications equipment. The AP1011 chip provides the crucial link that allows HyperTransport technology-based systems to use PCI (Peripheral Component Interface) devices that are currently on the market and under development.

The AP1011 provides the critical function of connecting the HyperTransport bus on microprocessors, network processors and ASICs (Application Specific Integrated Circuits) to a wide variety of PCI devices and peripherals. The chip connects the processors to hundreds of PCI chips for graphics, networking, mass storage, SCSI, among other purposes, and the new device can work with processors featuring HyperTransport in development from such companies as AMD, Broadcom Corporation, PMC-Sierra, Nvidia and SandCraft Inc.

"The industry needs to upgrade its I/O interconnect standards to keep up with the growing demands that faster processors and faster I/O devices place on system buses," said Nathan Brookwood, principal analyst at Insight 64. "Conventional parallel buses are reaching their practical performance limits, so a conversion to some form of high-speed serial technology is inevitable. HyperTransport technology offers a promising solution to this problem, and I anticipate that products like API NetWorks' AP1011 will play a key role in bridging the industry's transition to these new serial architectures."

This chip introduction is a significant step in API NetWorks' strategy to proliferate the adoption of HyperTransport in its move toward industry standard. API NetWorks is currently licensing intellectual property to the industry's leading hardware vendors in the form of the HyperTransport physical interface and protocols for the design of custom chips and ASICs.

"HyperTransport technology meets the need within the computing and networking industries for an advanced I/O interconnect to enhance the performance of their hardware," said Gabriele Sartori, director of technology evangelism at AMD. "With industry support already intensifying, API NetWorks chip development and the licensing of its intellectual property moves us closer toward the goal of making HyperTransport technology a standard for the industry."

"As co-developers of the technology, we have an excellent understanding of the HyperTransport bus and its protocols and have developed an aggressive product roadmap and intellectual property licensing program to proliferate the use of the technology," said David Rich, general manager of API NetWorks' HyperTransport business. "The AP1011 chip is a milestone product for the HyperTransport market, and API NetWorks is working closely with its partners to deliver real solutions based on this chip and HyperTransport by the beginning of next year."

HyperTransport technology (formerly LDT) moves data from processors to peripherals at speeds up to 60 times faster than a PCI bus (32-bit bus operating at 66 MHz) and is expected to improve the performance of a variety of computing and networking devices, including PCs, workstations, servers, Internet routers, optical switches, enterprise networks, central office equipment and cellular base stations.

Key to AP1011 chip and HyperTransport technology-based systems:

- AP1011 connects HyperTransport to a wide range of devices and peripherals
- Device maintains software compatibility
- HyperTransport bus is 1 Gbyte/s each way
- PCI is four 33MHz slots or two 66MHz slots
- AP1011 supports both 32-bit and 64-bit operation of its PCI bus
- Bus speeds can be set to the standard transfer speeds of 25, 33, 50 and 66 Mhz
- AP1011 is fully compliant with rev 2.2 of the PCI specification
- Up to 15 AP1011 devices can be daisy-chained to build higher-capacity systems with multiple PCI buses

Availability and Price

The AP1011 is currently sampling, with production in June. The device is priced at \$95 in a 352-pin SBGA (Super Ball Grid Array) in quantities of 1,000.

The company is also licensing its HyperTransport interface for its design into custom chips and ASICs. This intellectual property is licensed as a HyperTransport PHY (i.e., hard macro physical layer), and a RTL (Register Transfer Language) core that contains the HyperTransport protocols.

Additional information about API NetWorks' AP1011, its HyperTransport product development, intellectual property licensing program or HyperTransport technology is available at www.api-networks.com/silicon.

About API NetWorks, Inc.

API NetWorks, Inc. (formerly Alpha Processor, Inc.), a private company based in Concord, Massachusetts funded by Samsung Electronics Co., LTD. and Compaq Computer Corp, addresses the demand for bandwidth and time-to-market requirements in the electronics industry. API NetWorks' high-performance, high-density component technologies are ideal for markets such as network infrastructure, telecommunications, PCs, workstations, servers, among others. API NetWorks also leads the development of high-performance, high-density server and component technologies ideal for today's high-performance computing (HPC) and Internet markets. Additional information about API NetWorks and its complete product line can be accessed on the World Wide Web at www.api-networks.com.

About HyperTransport[®] Technology

HyperTransport is the industry's lowest latency, highest-performance, fully scalable, packet-based interconnect technology serving a wide range of industry segments. It is based on two 2-line to 32-line, asymmetric Low Voltage Differential Signaling (LVDS) links delivering up to 22.4 Gigabytes/second of aggregate CPU to CPU, CPU to I/O bandwidth in a highly efficient point-to-point, daisy-chain topology that replaces complex multi-level, multi-line buses. By enabling system designers to link peripheral subsystems or processors directly to the CPU or to multiple symmetric CPUs, the HyperTransport HTX[®] connector makes compute intensive, leading edge CPU-to-I/O and board-to-board designs a reality for server clustering and high performance peripheral applications. HyperTransport technology is embedded in multiple CPU families from AMD, Broadcom, IBM, PMC-Sierra and Transmeta and in a variety of semiconductors and IP cores. It is fully software-compatible with legacy Peripheral Component Interconnect (PCI), PCI-X and PCI Express technologies.

HyperTransport technology has been deployed in tens of millions of devices used in market leading products such as the Microsoft Xbox, Cisco routers, Apple, HP & Sun workstations, Apple, IBM, HP & Sun servers, HP blade PCs, HP & Sharp notebooks, Cray & IBM supercomputers, and all PCs, servers & cluster workstations based on the AMD Athlon[®] 64, the AMD Opteron[®] and Transmeta Efficeon processors. 2004 industry estimates from market analyst firm InStat project HyperTransport-based system product shipments to have reached nearly 26 million units in 2004 and to exceed 60 million units in 2006.

Specifications, overviews and white papers about HyperTransport technology can be found at www.hypertransport.org/tech/index.cfm.

About the HyperTransport[®] Technology Consortium

The HyperTransport Technology Consortium is a membership-based, non-profit organization in charge of managing and promoting HyperTransport Technology. It consists of over 40 industry-leading member companies, including founding members Advanced Micro Devices, Inc., Alliance Semiconductor, Apple Computer, Broadcom Corporation, Cisco Systems, NVIDIA, PMC-Sierra, Sun Microsystems, and Transmeta. Membership is based on a reasonable yearly fee and it is open to any company interested in licensing the royalty-free use of HyperTransport technology and intellectual property. Consortium members have full access to HyperTransport technical documents database, they may attend Consortium meetings and events and may benefit from a variety of technical and marketing services, including the new, member-driven web portal, whose business benefits are part of a wide array of services offered by the Consortium free of charge to member companies. To learn more about member benefits and on how to become a Consortium member, please visit the Consortium Web site at www.hypertransport.org/consortium/cons_join.cfm.

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